

Appn No. 10/043,763

Amdt date August 5, 2004

Reply to Office action of June 7, 2004

Amendments to the Specification:

Please replace the paragraph beginning on page 12, line 3 through page 15, line 22 through page 16, line 4, with the following rewritten paragraph:

As an example, assume that V_{DD0} is initially zero volts. Zero volts at the gate of device 1209 turns it on. In such case point 1211 charges to a potential close to the pad voltage, since device 1213 is off. Point 1211 is connected to the gate of device 1214 thereby turning device 1214 off. Since V_{DD0} is zero volts, PMOS device 1219 turns on, which causes the gate of device 1207 to be coupled to Bias_Mid. When the gate of device 1207 is coupled to Bias_Mid, device 1207 turns on. Device 1207 turning on couples V_{PAD} minus the threshold voltage of devices 1201, 1203, 1205 and 1207 to Bias_Mid. When V_{DD0} is low, device 1215 provides a ~~current leakage coupling~~ path for Bias_Mid to V_{DDC} or V_{DDP} . When V_{DD0} is low, the string of devices 1217 turns on and the pad voltage is coupled to Bias_Mid. Devices 1220, 1221, 1223 and 1225 act as protection for device 1209 in the instance where the V_{PAD} is high and V_{DD0} is low.